CLAIMS:

1. An apparatus for amplitude and phase modulation of a signal comprising:

a reference pulse oscillator arranged to provide a signal in the form of a series of input pulses;

an input for input modulating data including desired amplitude and phase modulation;

a vector logic circuit responsive to the input modulating data;

two digital delay lines each coupled to said reference oscillator and each having multiple delay cells for selectively delaying respective pulses of said signal;

two lookup tables each of which contains information for controlling the delay cells of a respective one of the delay lines so that the vector logic circuit controls an overall delay of the respective one of the digital delay lines using the information so as to generate therefrom a component vector which is dependent upon the input modulating data;

and a summer that is coupled to the two digital delay lines and arranged to combine together the component vectors from both of the delay lines to provide an output vector.

2. The apparatus according to Claim 1 wherein said vector logic circuit is arranged to utilize the desired amplitude and phase modulation to determine the phase of the two fixed magnitude component vectors.

3. The apparatus according to Claim 2 wherein the formula $\pm\text{Cos}^{-}$

$^{1}[r/(2V)]$ governs the phase offset of the component vectors from the desired output phase, where, in the governing formula, r represents the desired output magnitude and V is the magnitude of the component vectors.

4. The apparatus according to Claim 2 wherein said component vectors are assumed to have the same magnitude and be equidistant, radially, from the resultant vector.

5. The apparatus according to Claim 1 wherein said vector logic circuit is arranged to compensate for the special cases where the phase of leading or trailing vectors crosses the 360° barrier, where compensation is accomplished by either adding or subtracting 2π from the absolute phase of the vector.

6. The apparatus according to Claim 1 wherein said vector logic circuit is arranged to convert said phase modulation into an equivalent delay.

7. The apparatus according to Claim 6 wherein said vector logic circuit is arranged to update the lookup tables with the information required to reproduce the required delay.

8. The apparatus according to Claim 1 wherein said delay lines contain a number of sequential or parallel delay cells capable in combination of covering 360° of phase.

9. The apparatus according to Claim 8 wherein said delay cells have equivalent or weighted delay periods.

10. The apparatus according to Claim 1 wherein said delay lines contain a finite number of additional delay cells for the purpose of compensation in the range of the finest resolution step.

11. The apparatus according to Claim 1 wherein said delay cells contain a feedback edge detector whereupon detection of a falling edge enables the delay cell to confirm its next status from a lookup table.

12. The apparatus according to Claim 1 wherein said lookup tables contain the information required to reproduce a specified delay.

13. The apparatus according to Claim 1 wherein said lookup tables are directly referenced by the digital delay lines in order to control which delay cells are enabled at a given time.

14. The apparatus according to Claim 1 wherein said lookup tables contain redundant registers which contain both delay and compensation information.

15. The apparatus according to claim 1 wherein said digital delay lines generate component vectors of constant amplitude and wherein the summer is coupled to the two digital delay lines for the purpose of combining the two constant amplitude component vectors into a resultant vector containing a desired amplitude and phase.

16. The apparatus according to Claim 1 wherein said input pulses form a high power pulse train.

17. The apparatus according to Claim 1 in which the input for said input modulating data is digital such that digital data is converted into the output vector which is an analog signal, without the use of digital to analog converters.

18. The apparatus according to Claim 1 in which the input for said input modulating data is digital such that digital data is converted into the output vector which is an analog signal, and wherein the output vector is transmitted with

minimal amplification.

19. The apparatus according to Claim 1 in which the input for said input modulating data is digital such that digital data is converted into the output vector which is an analog signal, and wherein the output vector is amplified utilizing non-linear amplifiers.